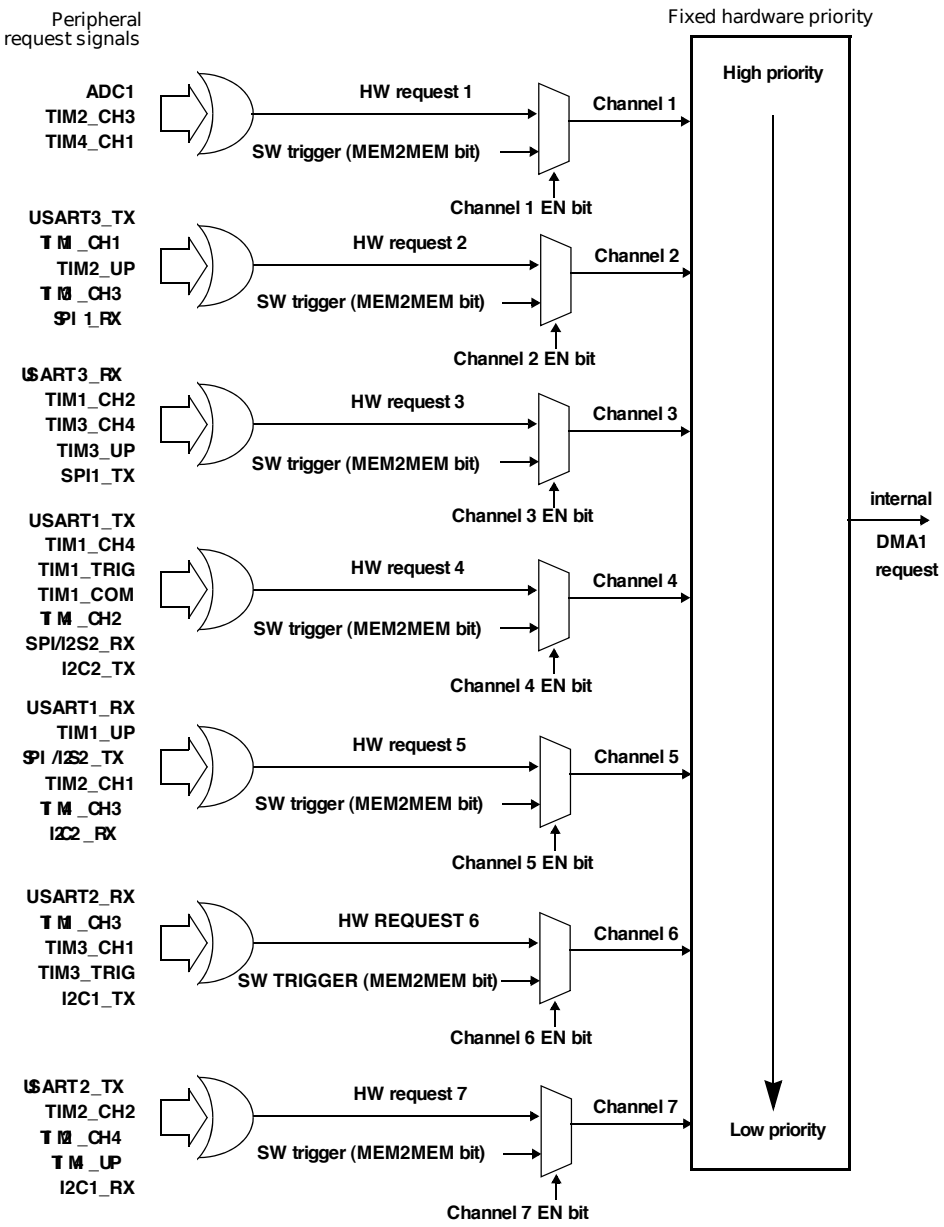
Peripheral request signals
Fixed hardware priority
High priority
Low priority
ADC1
TIM2_CH3
TIM4_CH1
HW request 1
SW trigger (MEM2MEM bit)
Channel 1
Channel 1 EN bit
USART3_TX
TIM1_CH1
TIM2_UP
TIM3_CH3
SPI1_RX
HW request 2
SW trigger (MEM2MEM bit)
Channel 2
Channel 2 EN bit
USART3_RX
TIM1_CH2
TIM3_CH4
TIM3_UP
SPI1_TX
HW request 3
SW trigger (MEM2MEM bit)
Channel 3
Channel 3 EN bit
USART1_TX
TIM1_CH4
TIM1_TRIG
TIM1_COM
TIM4_CH2
SPI/I2S2_RX
I2C2_TX
HW request 4
SW trigger (MEM2MEM bit)
Channel 4
Channel 4 EN bit
USART1_RX
TIM1_UP
SPI/I2S2_TX
TIM2_CH1
TIM4_CH3
I2C2_RX
HW request 5
SW trigger (MEM2MEM bit)
Channel 5
Channel 5 EN bit
USART2_RX
TIM1_CH3
TIM3_CH1
TIM3_TRIG
I2C1_TX
HW REQUEST 6
SW TRIGGER (MEM2MEM bit)
Channel 6
Channel 6 EN bit
USART2_TX
TIM2_CH2
TIM2_CH4
TIM4_UP
I2C1_RX
HW request 7
SW trigger (MEM2MEM bit)
Channel 7
Channel 7 EN bit
internal
DMA1
request